

WHAT IS CLAIMED IS:

1. A memory device comprising:

hysteretic capacitance means; and

5 a read circuit applying a bias voltage to said capacitance means in different directions in a first time and a second time of data reading respectively for defining read data by comparing first read data and second read data with each other.

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2. The memory device according to claim 1, wherein

said read circuit defines said read data on the basis of a variation of the potential of a bit line corresponding to said first read data and a variation of the potential of a bit line corresponding to said second read data.

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3. The memory device according to claim 2, wherein

said read circuit includes a first circuit part

20 detecting said variation of the potential of said bit line corresponding to said first read data and a second circuit part detecting said variation of the potential of said bit line corresponding to said second read data.

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4. The memory device according to claim 3, wherein

said first circuit part includes a first transistor connected to said bit line for entering an ON state in said first time of said data reading and entering an OFF state in said second time of said data reading, and

5 said second circuit part includes a second transistor connected to said bit line for entering an ON state in said second time of said data reading and entering an OFF state in said first time of said data reading.

10 5. The memory device according to claim 1, wherein said read circuit includes a resistance dividing circuit for generating a reference potential consisting of a first potential.

15 6. The memory device according to claim 5, wherein said read circuit defines said read data on the basis of the difference between a variation of the potential of a bit line corresponding to said first read data and a variation of the potential of a bit line corresponding to
20 said second read data and said reference potential consisting of said first potential generated by said resistance dividing circuit.

25 7. The memory device according to claim 6, wherein said read circuit includes a comparator comparing the

difference between said variation of the potential of said
bit line corresponding to said first read data and said
variation of the potential of said bit line corresponding
to said second read data and said reference potential
5 generated by said resistance dividing circuit with each
other.

8. The memory device according to claim 7, wherein
said comparator includes a first input terminal
10 supplied with said reference potential and a second input
terminal connected with a node,

said resistance dividing circuit also generates a
second potential in addition to said reference potential
consisting of said first potential, and
15 said second potential is applied to said node
connected with said second input terminal of said
comparator as an initial potential.

9. The memory device according to claim 8, wherein
20 said read circuit includes a third transistor
connected between a portion of said resistance dividing
circuit generating said second potential and said node
connected with said second input terminal of said
comparator for entering an ON state in an initial state
25 and entering an OFF state in said data reading.

10. The memory device according to claim 8, wherein
said reference potential is set to an intermediate
level between a potential obtained by adding the
5 difference between said variation of the potential of said
bit line corresponding to said first read data and said
variation of the potential of said bit line corresponding
to said second read data with reference to initial data
formed by first data to said initial potential of said
10 node and a potential obtained by adding the difference
between said variation of the potential of said bit line
corresponding to said first read data and said variation
of the potential of said bit line corresponding to said
second read data with reference to initial data formed by
15 second data to said initial potential of said node.

11. The memory device according to claim 1, wherein
first said bias voltage and second said bias voltage
applied to said capacitance means in said data reading are
20 voltages, reversed in polarity to each other, having
substantially equal absolute values.

12. The memory device according to claim 1, wherein
the hysteresis curve of said capacitance means is
25 substantially symmetrical with respect to the origin.

13. The memory device according to claim 1, wherein
said hysteretic capacitance means includes a
ferroelectric capacitor.

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14. The memory device according to claim 13, wherein
said ferroelectric capacitor consists of a bit line,
a word line and a ferroelectric film arranged between said
bit line and said word line,

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said memory device further comprising memory cells
each consisting of said ferroelectric capacitor.

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15. The memory device according to claim 14, wherein
a voltage n/m times said bias voltage, where $m > n$,
is applied to memory cells other than selected said memory
cell in said data reading.

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16. The memory device according to claim 13, further
comprising memory cells each consisting of a single said
ferroelectric capacitor and a single transistor connected
to said ferroelectric capacitor.